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Research Article

A Novel Fault-Tolerant Majority Gate Architecture for Robust Operation in QCA-Based Nano Circuits

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Abstract: Quantum Dot Cellular Automata (QCA) is one of the promising alternatives to the traditional CMOS technologies for next-generation nanocomputing, which can be integrated at a higher density and has a higher possibility of low power consumption. Fabrication defects, environmental noise, and fault tolerance, especially in larger circuits, are challenging for practical implementation of QCA circuits. A new Fault-Tolerant Majority Gate (FTMG) is presented in this paper. This work analyzes various defects that can occur in the Majority Gate (MG) and then compares the fault tolerant majority gates based on the number of cells in the device, defect types and the degree of fault tolerance. This design of majority gate is simulated using QCADesigner 2.0.3. This paper focuses on the analysis of missing cells and displacement defects. The proposed majority gate is analyzed for both defects, and the full adder and decoder circuits are designed using the proposed MG.

Keywords: Fault Tolerance, Majority Gate (MG), Quantum Dot Cellular Automata (QCA), Single Missing Cell Defects (SMCD), Double Missing Cell Defects (DMCD)

Introduction

One of the key factors in the evolution of computers has been Moore's law, which predicts that the number of transistors that will fit on a chip double roughly every 18 months. But the current CMOS technology is being constrained by physical scaling of transistors. As transistors are smaller, they become more difficult to control and are prone to leakage, which can lead to increased power consumption and heat generation. Therefore, alternative technologies are needed to replace CMOS technology. While quantum computing and nano-scale logic paradigms are gaining attention, the practical realization of reliable QCA circuits remains a major challenge due to defect sensitivity, making fault-tolerant design a critical research direction.

Quantum Dot Cellular Automata (QCA) represents a revolutionary concept in digital computing, where binary information is encoded in the configuration of charge in quantum dots. Compared to conventional CMOS-based circuits, QCA is far more energy-efficient because it does not require current flow to function. We reviewed numerous papers that demonstrate the implementation of basic logic gates using QCA technology (Walus et al., 2005; Almatrood et al., 2021). Furthermore, several studies illustrate the design of combinational logic circuits such as XOR gates (Salih et al., 2022; Goswami et al., 2017; Repe and Koli, 2023a), decoders (Ratna et al., 2021), and full adders (Goswami et al., 2017) using QCA. Some research also explores the realization of sequential circuits with QCA implementations (Repe and Koli, 2023b). However, QCA circuits are susceptible to errors due to noise, fabrication imperfections, and various environmental factors. Several studies have investigated different types of defects and their impact at the logic level (Tahoori et al., 2004). Additionally, fault analysis has been conducted on combinational circuits, including the half adder, to assess their reliability under such conditions (Dhare and Mehta, 2015). The majority gate is the fundamental building block of QCA-based logic circuits and is essential for implementing basic logic gates such as NAND, NOR, NOT, and XOR. QCA technology offers the advantage of low power consumption. One of the primary challenges in developing larger and more complex QCA systems is ensuring fault tolerance and reliability. To address this, the design of Fault Tolerant Majority Gate (FTMG) becomes crucial for the successful realization of robust digital circuits. Several fault-tolerant

majority gate (FTMG) designs have been explored in the literature (Farazkish et al., 2012; Du et al., 2016; Taheri et al., 2019; Foroutan et al., 2021; Wang et al., 2018; Dalui et al., 2010; Mehta and Dhare, 2017; Singh et al., 2018), with specific attention given to tolerance against multiple missing cell defects (Dhare and Mehta, 2018) and displacement defects.

Although significant progress has been made in QCA-based logic circuit design, existing fault-tolerant majority gate structures suffer from an inherent tradeoff between hardware complexity and reliability. Designs with fewer QCA cells exhibit poor fault tolerance, particularly under multiple missing cell defects, whereas highly fault-tolerant designs require many cells, leading to increased area and design complexity. Moreover, displacement defect tolerance has not been sufficiently addressed in existing literature, despite being a critical issue in nanoscale fabrication.

To overcome these limitations, this paper proposes a novel Fault-Tolerant Majority Gate (FTMG) architecture that achieves a balanced optimization between cell count, area, and fault tolerance. The proposed design not only reduces the number of device cells compared to highly redundant structures but also demonstrates high resilience against single and double missing-cell defects, along with 100% fault tolerance under displacement defects, which is not commonly reported in prior works.

The key contributions of this work are as follows:

- A fault-tolerant QCA majority gate design with improved defect resilience
- Reduced and optimized cell structure compared to existing designs
- Balanced trade-off between fault tolerance and cell count
- Robust performance under missing cell and displacement defects
- Implementation of a full adder and decoder to validate practical usability
- Comparative analysis with existing QCA majority gate designs

QCA Cell Structure

The basic structure of the Quantum-dot Cellular Automata (QCA) cell is four quantum dots placed at the corner of a square. The dimensions of the cells in a QCA are 18nm x 18nm, and the spacing between cells is 2nm. Within a cell, two electrons are typically confined, at the corners of the cells, always diagonally due to interacting via Coulombic repulsion. Such electrons can hop freely between the quantum dots but are blocked from escaping from the cell. The inter-electron repulsion dictates the cell's polarization. The two stable electron configurations, representing binary states, arise from the electrons positioning themselves diagonally opposite to minimize their electrostatic repulsion. These two configurations are denoted as: Polarization +1: When the electrons occupy one diagonal pair of quantum dots, this state represents a logical '1'. Polarization -1: When the electrons occupy the other diagonal pair, this state represents a logical '0' (Lent et al., 1993; 2002) as shown in Fig. 1.

Polarization is calculated via Eq:

$$P = \frac{(\rho 1 + \rho 3) - (\rho 2 + \rho 4)}{\rho 1 + \rho 2 + \rho 3 + \rho 4} \quad (1)$$

Here, P is the charge of the i^{th} quantum dot cell ($\rho = 1$ if an electron is present; otherwise, it is 0). These polarizations are represented by logic-0 and logic-1 (in other words, binary 0 and binary 1) (Lent et al., 1993; 2002; Chetti and Yatgal, 2022; Askari and Taghizadeh, 2011; Foroutan et al., 2021; Walus et al., 2005; Almatrood et al., 2021; Salih et al., 2022; Goswami et al., 2017; Repe and Koli, 2023a; Ratna et al., 2021).

Qca Wire, Inverter and Majority Gate

The transfer of logic data in QCA is realized by the coulombic interaction between the electrons of neighboring cells. Series the binary wire is made up of QCA cells and is the simplest QCA circuit. The wire arrangement of QCA cells is as shown in Fig. 2.

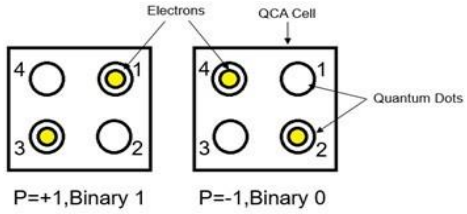


Fig. 1: QCA cell Structure with polarization

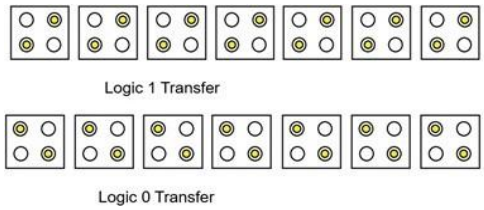


Fig. 2: Binary wire with cell orientation 90

45-Degree (Diagonal) Wire: There are two possible alignments for QCA cells:" Standard" and" Rotated." In the Standard alignment, the cells are arranged at a 90° angle, while in the Rotated alignment, the cells are placed at a 45°. (Chetti and Yatgal, 2022; Askari and Taghizadeh, 2011; Foroutan et al., 2021; Walus et al., 2005; Almatrood et al., 2021; Salih et al., 2022; Goswami et al., 2017; Repe and Koli, 2023a-b; Ratna et al., 2021; Tahoori et al., 2004; Dhare and Mehta, 2015; Farazkish et al., 2012; Du et al., 2016; Taheri et al., 2019; Foroutan et al., 2021; Wang et al., 2018; Dhare and Mehta, 2018; Tóth and Lent, 2001).; Rahimi and Estiri, 2024). The wire with rotated cells is shown in Fig. 3.

QCA Clock

Clocking is a fundamental aspect of QCA circuits, playing a role significantly different from that in traditional CMOS designs. In QCA, a clock is not merely used for synchronization; it is essential for controlling the flow of information and, crucially, for providing the power required to operate the circuit. QCA computation is achieved by manipulating the tunneling of electrons between quantum dots within the cells, and this process is precisely governed by a multi-phased clock signal. The primary purposes of the QCA clock are twofold: To supply the energy needed for computation within the automaton and to dictate the direction in which data flows through the circuit. This control over data flow is realized by modulating the potential barriers that exist between adjacent quantum dots within the QCA cells.

The clocking mechanism in QCA is shown in Fig. 4, which typically employs a four-phase signal to control the state and interaction of the quantum dot cells. These four phases, usually referred to as Switch, Hold, Release, and Relax, occur sequentially and are crucial for the proper operation and pipe-lined nature of computation in QCA circuits. A typical QCA design utilizes four clock signals, each cyclically shifted by 90 degrees relative to the preceding one. This phase lag ensures a controlled and directional flow of data through the circuit. (Askari and Taghizadeh, 2011).

Fig. 3: Binary wire with cell orientation 45

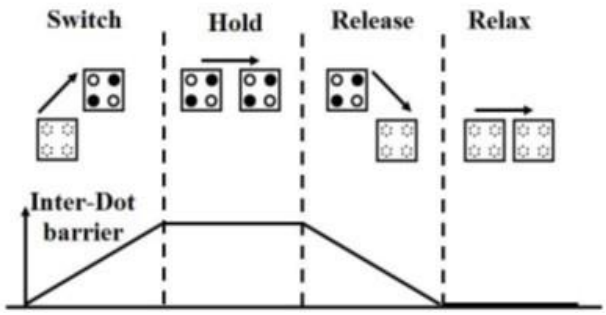
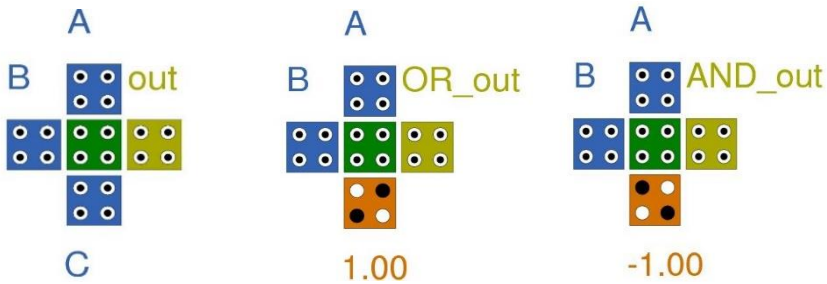


Fig. 4: Four Clock Phases of QCA clock (Askari and Taghizadeh, 2011)

Majority Gate

A Majority Gate (MG) in Fig. 5(a) is a fundamental logic gate in QCA that computes the majority function, which determines the most common value among three or more inputs. It plays a crucial role in QCA circuits (Mehta and Dhare, 2017), as it can be used to implement AND logic, OR logic, and other logic functions. The three-input majority gate circuit is shown in Fig. 5. The majority gate follows the function: $M(A, B, C)=AB+BC+CA$. When at least 2 inputs are 1, the output is 1, and when two inputs are 0, the output is 0. We can design an AND gate by applying one of the inputs to 0(here for QCA polarization 1). In Fig. 5(b), input C is given polarization -1, and it works as an AND gate. Similarly, input C is applied to polarization 1, then the majority gate operates as an OR gate (Fig. 5(c)). The majority gate Truth table is as shown in Table 1.



(a) Majority Gate (MG) b) OR Logic (c) AND Logic

Fig. 5: Majority Gate, AND Gate, OR Gat

Table 1: Truth table of Majority Gate $M(A, B, C)=AB+BC+CA$

A	B	C	M (A, B, C)
o	o	o	o
o	o	1	o
o	1	o	o
o	1	1	1
1	o	o	o
1	o	1	1
1	1	o	1
1	1	1	1

Inverter Using QCA

Not Gate (Inverter) design is also a basic gate to build the Universal gate like NAND and NOR. Fig. 6 shows the QCA based inverter design with input set to logic 1(polarization -1) and output obtain is logic 0, which is shown in simulation result.

Defect Analysis of Majority Gate

Manufacturing imperfections, as depicted in Fig. 7, can introduce various defects into QCA cells and circuits. To minimize these issues and enhance reliability, fault-tolerant circuits are essential in QCA designs. This inherent ability to withstand defects strengthens QCA's potential as a replacement for CMOS technology. This study focuses on the analysis of missing cell defects, with particular emphasis on single and double missing cell defects. It presents a comparative evaluation of various FTMG designs in addressing these defects, providing insights into their effectiveness and reliability. Fault tolerance of QCA circuit can be calculated by ratio of number of correctly functioning cells to total number of cells in the circuit. A higher Fault Tolerance Ratio indicates better fault tolerance.

Fault tolerant Majority Gate (FTMG)

A Fault-Tolerant Majority Gate (FTMG) utilizing 13 QCA cells is designed, as illustrated in Fig. 8(a) Farazkish et al., 2012). The structure comprises nine central cells, input cells A, B, and C, and a single output cell (Output). The polarization of the input cells remains fixed, while the central and output cells are free to switch states. The device cells are sequentially labeled from 1 to 9, as shown in Fig. 8(b).

The impact of a single missing cell defect was analyzed using QCA Designer. Simulation results indicate that when cell numbers 1, 3, 5, 7, or 9 are missing, the majority gate continues to produce the correct output. However, if cell numbers 2, 4, 6, or 8 are missing, the majority gate fails to generate erroneous output. For a single missing cell defect, the majority gate (Farazkish et al., 2012) demonstrates a fault tolerance of 55.6%, indicating that it remains functional in 55.6% of defect scenarios.

If any two cells are missing from the nine device cells, the possible missing cell combinations can be determined using the binomial coefficient nCr, where n = 9 (total device cells) and r = 2 (missing cells). All possible combinations are illustrated in Table 2. Among the 36 possible missing cell combinations, 6 combinations (highlighted in yellow) produce the correct output, while the remaining 30 combinations result in an erroneous output. For a double missing cell defect, the majority gate (Farazkish et al., 2012) demonstrates a fault tolerance of 16.67%, indicating that it remains functional in 16.67% of defect scenarios, which is very less. The Majority Gate (MG) design shown in Fig. 9 (Du et al., 2016) consists of 19 QCA cells, including three input cells, one output cell, and 15 device cells. To evaluate its robustness, we analyzed its behavior under Single Missing Cell Defects (SMCD). Among the 15 device cells, 9 missing cell cases produced correct outputs, while 6 resulted in erroneous outputs, yielding a fault tolerance ratio of 60%.

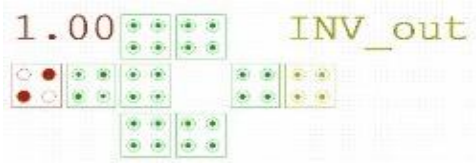


Fig. 6: Inverter (NOT Gate)

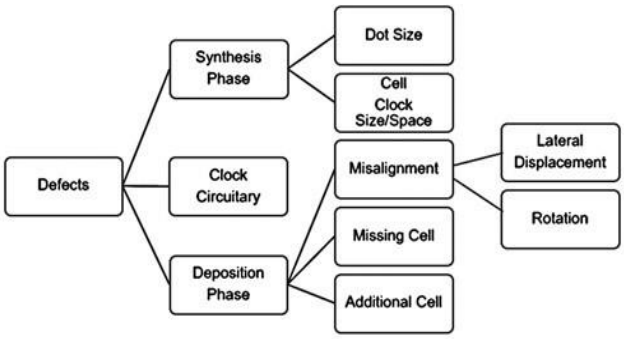


Fig. 7: Defects in QCA (Chetti and Yatgal, 2022)

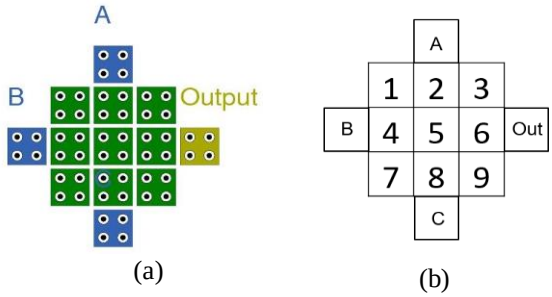


Fig. 8: Fault-tolerant majority gate (FTMG) (Farazkish et al., 2012)

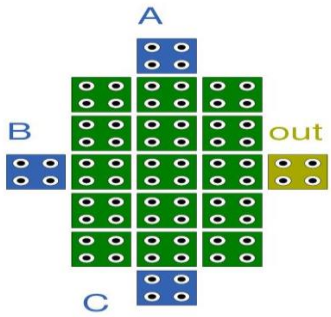


Fig. 9: Fault-tolerant majority gate (Du et al., 2016)

For Double Missing Cell Defects (DMCD), the total number of possible defect combinations is determined using the binomial coefficient nCr, where n = 15 (device cells) and r = 2 (missing cells). This results in 105 possible defect scenarios, out of which 33 configurations maintained correct functionality, leading to a fault tolerance of 31.4%.

These results demonstrate the circuit's resilience against SMCD and DMCD, providing valuable insights into its fault tolerance capabilities. The Majority Gate (MG) design presented in Fig. 10 (Taheri et al., 2019) consists of 16 device cells, along with input cells A, B, C, and output cell (Cout). During the single missing cell defect analysis, it was observed that the gate produces the correct output for 10 out of 16 missing cell cases, while the remaining 6 cases result in erroneous outputs. This corresponds to a fault tolerance of 62.5%.

For Double Missing Cell Defects (DMCD), the total number of possible defect patterns is determined using the binomial coefficient, where n = 16 (device cells) and r = 2 (missing cells), yielding 120 possible defect scenarios. Among these, the circuit maintains correct functionality in 45 cases, resulting in a fault tolerance of 37.5%.

The majority gate (MG) design illustrated in Fig. 11 (Foroutan et al., 2021) comprises 33 device cells, along with input cells A, B, C, and output cell (Cout).

During the Single Missing Cell Defect (SMCD) analysis, the gate exhibited correct functionality in 28 out of 33 cases, while the remaining 5 cases resulted in erroneous outputs, leading to a fault tolerance of 84.84%.

For DMCD, the total number of possible defect combinations is computed using the binomial coefficient, where n = 33(device cells) and r = 2 (missing cells), resulting in 528 possible defect scenarios. Among these, the circuit successfully maintained correct operation in 317 cases, corresponding to a fault tolerance of 60.03%. The majority gate design shown in Fig. 12 (Wang et al., 2018) comprises 32 device cells, along with input cells A, B, C, and output cell (OUTPUT).

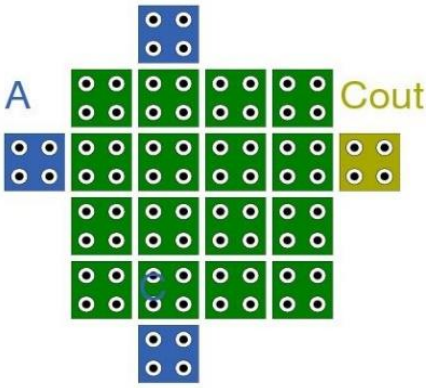


Fig. 10: Majority Gate design (Taheri et al., 2019)

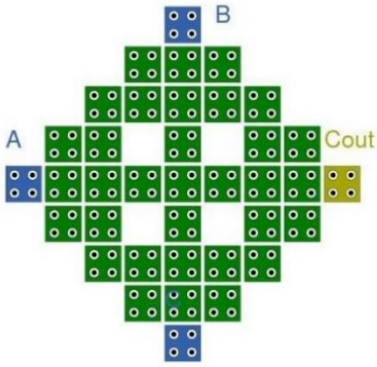


Fig. 11: Majority Gate design (Foroutan et al., 2021)

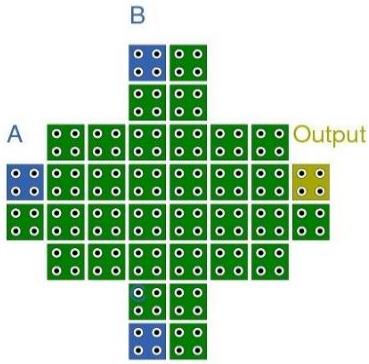


Fig. 12: Fault-tolerant Majority gate (Du et al., 2016)

During the single missing cell defect analysis, it was observed that the gate produced the correct output in 30 out of 32 cases, while the remaining 2 cases led to erroneous outputs, resulting in a fault tolerance of 93.8%.

For Double Missing Cell Defects (DMCD), the circuit demonstrated a fault tolerance of 66.7%. These findings underscore the circuit's high resilience against SMCD and DMCD, making it a robust option for QCA-based logic design.

Proposed Fault-Tolerant Majority Gate

Fig. 13(a) illustrates the proposed fault-tolerant Majority Gate (MG), which comprises 29 device cells, input cells A, B, C, and output cell (OUTPUT). The device cells are individually numbered, as depicted in Fig. 13(b). The fabrication of nanoscale devices is often susceptible to various types of defects. In this study, we focus on evaluating the performance of the proposed Majority Gate (MG) design, considering missing cell defects, specifically single and double missing cells, and cell displacement defects. The number of QCA cells is optimized to maintain a balance between fault tolerance and hardware complexity. Excessive increase in device cells may improve fault tolerance but negatively impacts

area, power consumption, and clocking overhead. Therefore, the proposed design maintains an optimized structure with 29 cells to achieve reliable performance. Simulation result of MG is shown in Fig. 16.

Missing Cell Defect Analysis of Fault Tolerant Majority Gate (FTMG)

For SMCD analysis, it is observed that the output remains correct for all cases except when cell number 9 or 21 is missing. Results are shown in Table 3. This indicates that the design provides correct outputs in 27 out of 29 possible single cell fault cases, resulting in a fault tolerance of 93.10% for (SMCD).

In the case of double missing cell defects, all possible combinations of two missing cells out of the 29 device cells are considered. The total number of such combinations, computed using the binomial coefficient (n = 29, r = 2), is 406. Among these, faulty outputs were observed in 139 cases, as detailed in Table 2. Specifically, the output was stuck at logic level C in 61 cases, stuck at B in 12 cases, and stuck at A in 55 cases. Other faulty output types are also listed in Table 4. Consequently, the proposed majority gate design produced correct outputs in 267 out of 406 double cell fault scenarios, demonstrating its resilience to double missing cell defects. This provides fault tolerance for a double missing cell, 65.76%.

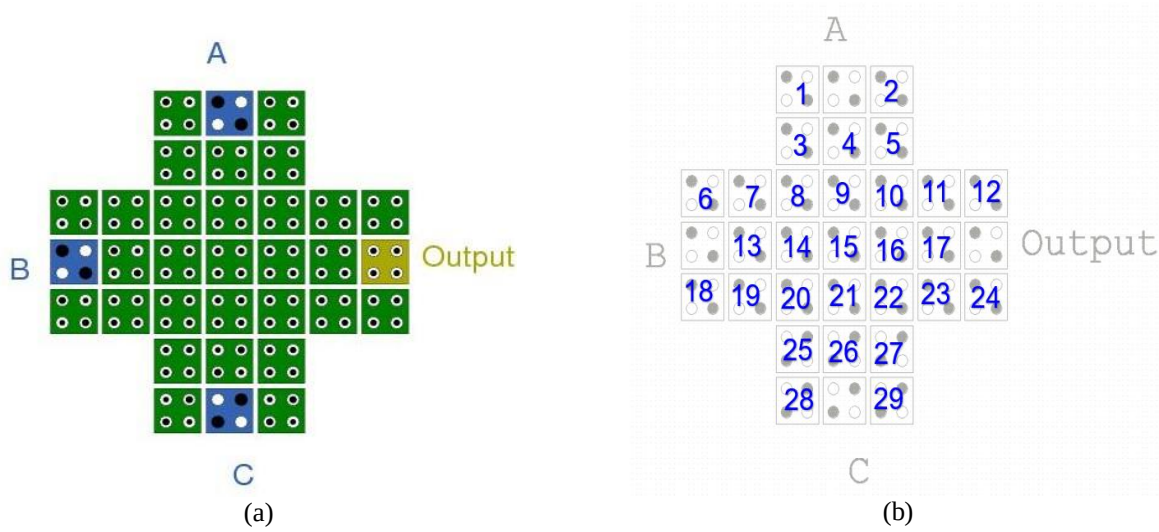


Fig. 13: Proposed Fault Tolerant Majority Gate (FTMG)

Table 2: All possible combinations for the double missing cell defect

1,2	2,4	3,7	5,7
1,3	2,5	3,8	5,8
1,4	2,6	3,9	5,9
1,5	2,7	4,5	6,7
1,6	2,8	4,6	6,8
1,7	2,9	4,7	6,9
1,8	3,4	4,8	7,8
1,9	3,5	4,9	7,9
2,3	3,6	5,6	8,9

Table 3: The majority gate output for a single missing cell defect (SMCD)

DeviceCellNo	Output	DeviceCellNo	Output	DeviceCellNo	Output	DeviceCellNo	Output
1	Correct	9	S–a-C	17	Correct	25	Correct
2	Correct	10	Correct	18	Correct	26	Correct
3	Correct	11	Correct	19	Correct	27	Correct
4	Correct	12	Correct	20	Correct	28	Correct
5	Correct	13	Correct	21	S–a-A	29	Correct
6	Correct	14	Correct	22	Correct		
7	Correct	15	Correct	23	Correct		
8	Correct	16	Correct	24	Correct		

Table 4: Double missing cell defect (DMCD)

Number of Cell pairs	Fault
61	S-a-C
12	S-a-B
55	S-a-A
1	ABC'+C
1	AC+ABC'
1	AC+A'BC
4	AB'+BC+ABC'
1	AC
1	A(B'C+BC') +BC
2	Undefined
267	M(A,B,C)

Displacement Defect Analysis of Fault Tolerant Majority Gate (FTMG)

Displacement defect analysis is carried out and it can be observed that cell no-1 in Fig.13(b) can be displaced in north or west directions only as, on its south, cell no 3 is located and on its east, input cell A is located, similarly cell A (input cell) can be displaced only in north direction. Table 5 shows the displacement defect tolerance of input and output cells. The results indicate the maximum allowable displacement range by which the majority gate continues to produce correct output. This demonstrates the robustness of the proposed design against fabrication-related displacement errors. Input cell A can be displaced in the north direction up to 8nm, resulting in a correct output, but if the displacement is beyond the limit, then we get an erroneous output. Similarly, cell B can be displaced in the west direction up to 9nm without loss of output. Displacement of cell C in south up to 8nm resulting in correct output, but beyond this limit erroneous output is obtained. Except for input cells, no effect of any other cell displacement can be seen in the output result, so we can say 100% fault tolerance for cell displacement defect is obtained in this design. Cell 4,8,9,10,13,14,15,16,17,20,21,22,26 are not considered for cell displacement defect as they are surrounded by other cells in all four directions, so there is no scope of displacement of these cells in the design.

Full Adder Design Using Fault-Tolerant Majority Gate (FTMG)

The complete circuit implementation utilizing the proposed majority gate is illustrated in Fig. 14. This design functions as a full adder, with three inputs: A, B, and C, and two outputs: Sum and Carry. The circuit operates using two clock zones Clock 0 and Clock 1 ensuring that the output is synchronized with Clock 1. The corresponding simulation results of the full adder outputs are presented in Fig. 17. Boolean equations for the full adder outputs are.

Decoder Design Using Fault-Tolerant Majority Gate

A decoder is an important building block in digital systems; it can be used to design multiplexers, control logic, memory addressing, and data routing. QCA based Decoder circuit is designed using fault tolerant proposed majority gate as shown in Fig. 15. Decoder inputs are A and B and outputs are D_0, D_1, D_2 and D_3. When both inputs A and B are 0, output D0 is 1. Truth table for decoder circuit is shown in Table 6. Simulation result for decoder is shown in Fig. 18. Decoder is designed using three clock zones, resulting in the output latency of 0.75 clock cycles.

$$Sum = A \oplus B \oplus C, Carry = M(A,B,C) \quad (3)$$

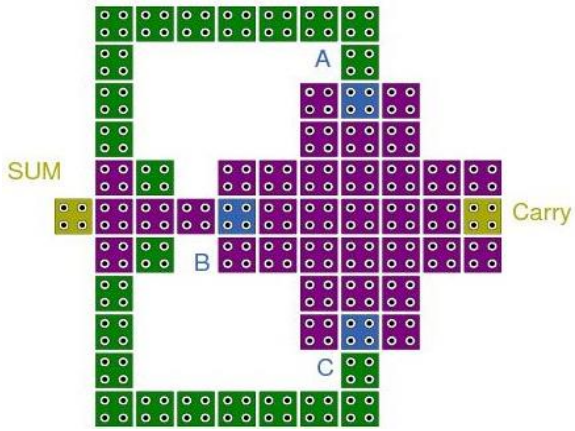


Fig. 14: Full adder design using proposed FTMG

Table 5: Displacement defect Analysis

cell	North	South	East	West	cell	North	South	East	West
A	8nm	–	–	–	12	∞	–	∞	–
B	–	–	–	9nm	18	–	∞	–	∞
C	–	8nm	–	–	19	–	∞	–	–
1	∞	–	–	∞	23	–	∞	–	–
2	∞	–	∞	–	24	–	∞	∞	–
3	–	–	–	∞	25	–	–	–	∞
5	–	–	∞	–	27	–	–	∞	–
6	∞	–	–	∞	28	–	∞	–	–
7	∞	–	–	–	29	–	∞	∞	–
11	∞	–	–	–	–	–	–	–	

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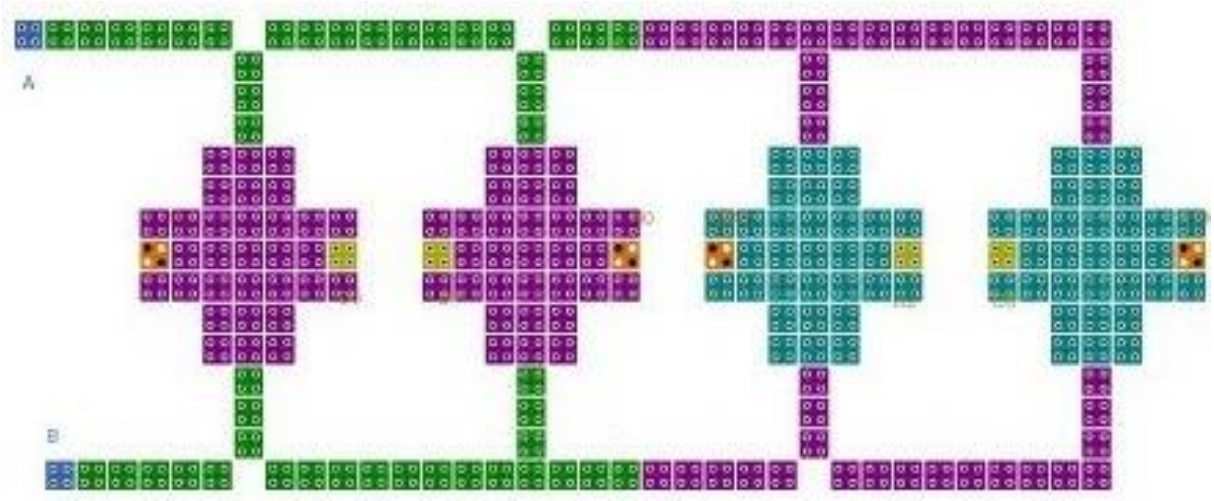

Fig. 15: Decoder design using FTMG

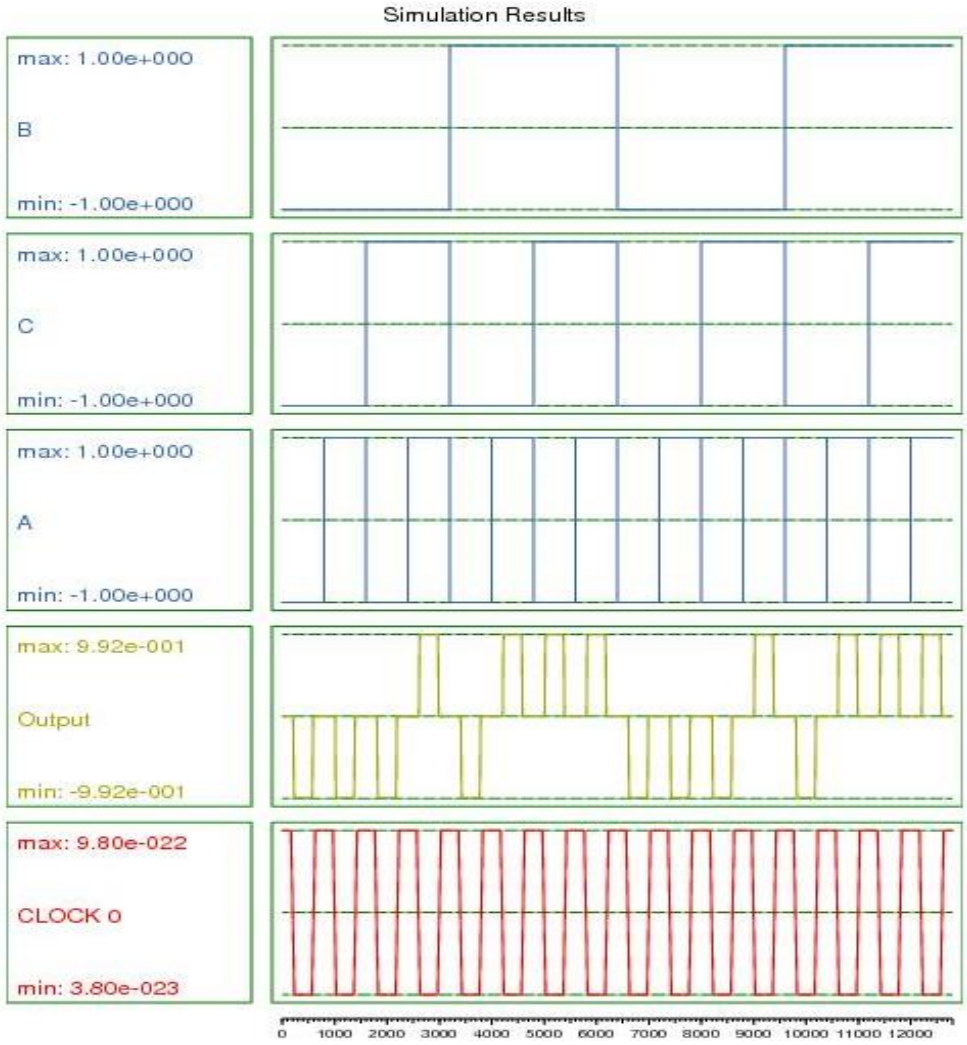

Fig. 16: Simulation result of Proposed FTMG

DOI: 10.3844/jcssp.2026.2118.2129

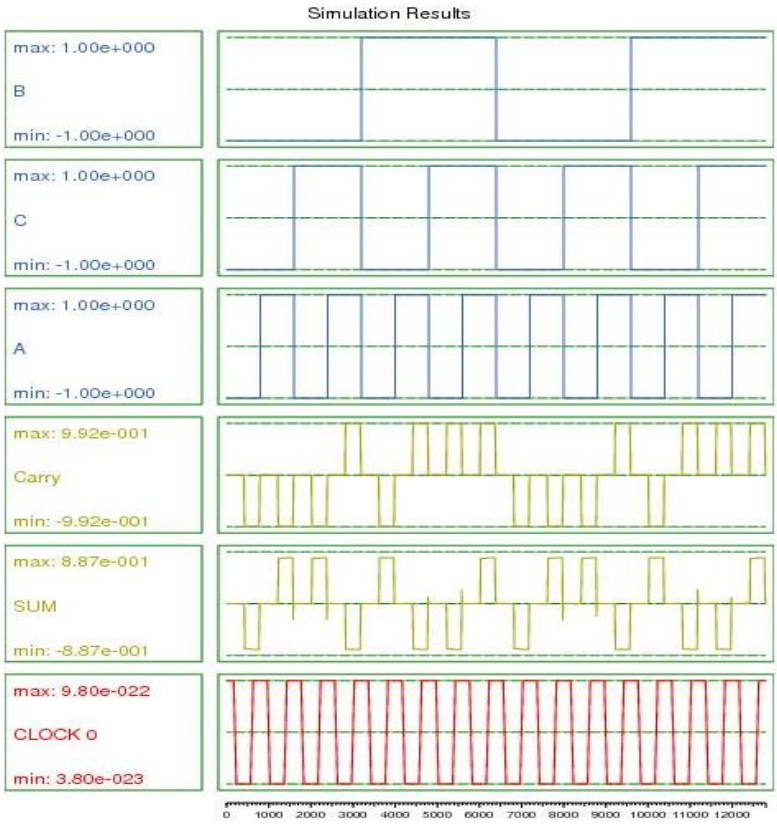

Fig. 17: Simulation results of the full adder designed using the proposed MG

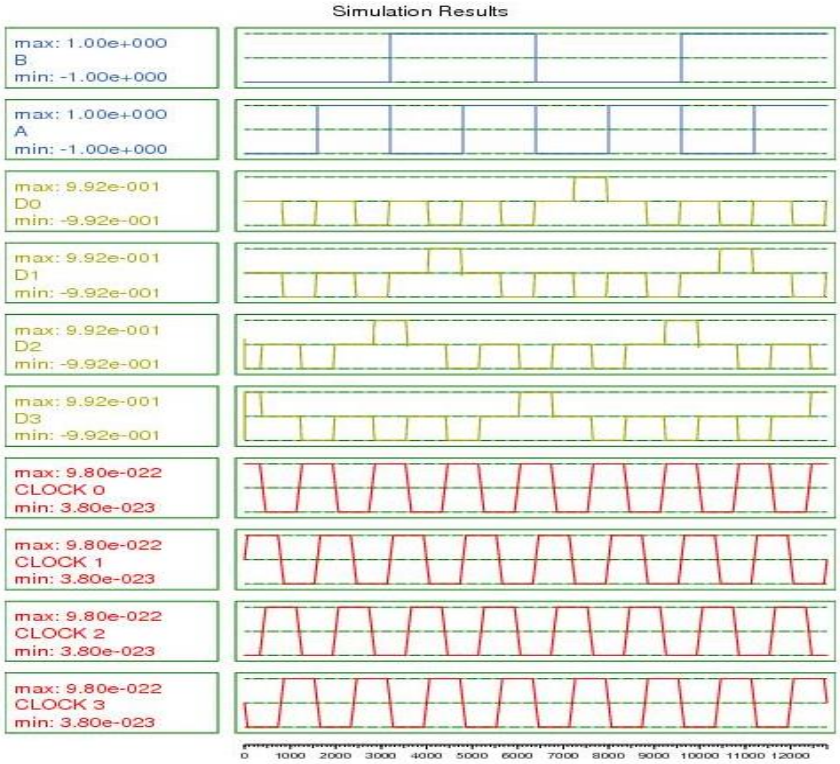

Fig. 18: Simulation result of Decoder

Table 6: Decoder Truth Table

A	B	D0	D1	D2	D3
o	o	1	o	o	o
o	1	o	1	o	o
1	o	o	o	1	o
1	1	o	o	o	1

Results and Discussion

Table 7 presents a comparative evaluation of the proposed majority voter against existing designs with respect to device cell count, fault tolerance, and area. Early implementations reported in Farazkish et al. (2012); Du et al. (2016); Taheri et al. (2019) employ fewer device cells and occupy a smaller area (0.02 μm²); however, their limited structural redundancy results in lower reliability. Designs in (Foroutan et al., 2021; Wang et al., 2018) improve fault tolerance by increasing the number of device cells beyond 32, at the cost of increased area (0.04 μm²). The proposed design uses 29 device cells with an area of 0.04 μm², indicating a more efficient use of redundancy.

Under single missing-cell fault conditions, (Farazkish et al., 2012; Du et al., 2016; Taheri et al., 2019) achieve fault tolerance values ranging from 55.6% to 62.5%. Higher redundancy designs in Foroutan et al. (2021); Wang et al. (2018) report 84.84% and 93.8% fault tolerance, respectively. The proposed design achieves a single missing-cell fault tolerance of 93.10%, comparable to the highest reported value, while requiring fewer device cells, demonstrating improved robustness against localized defects.

For double missing-cell faults, designs with low device counts exhibit tolerance below 40%, whereas (Foroutan et al., 2021; Wang et al., 2018) achieve 60.03% and 66.67%, respectively. The proposed design attains a fault tolerance of 65.76%, closely matching the best existing design with reduced structural complexity. These results indicate that the proposed majority voter provides a favorable trade-off between fault tolerance and hardware overhead, making it suitable for reliable QCA-based logic implementations. The results indicate that the proposed design is not merely an incremental structural modification, but a design level optimization that improves fault resilience without an increase in hardware cost. This demonstrates that careful cell placement and interaction can significantly enhance robustness in QCA circuits, which is critical for scalable nano computing architectures. The proposed majority gate exhibits lower energy dissipation due to optimized cell arrangement and reduced clocking overhead, making it suitable for low-power QCA implementations.

Table 7: Single missing cell and double missing cell defect Analysis

Majority Voter Design	No of Device Cells	Correct output for single cell missing	Fault tolerance for a single missing cell (%)	Fault tolerance for Double missing cell (%)	Area
Farazkish et al. (2012)	9	5	55.60	16.67	0.02 um^2
Du et al. (2016)	15	9	60.00	31.40	0.02 um2
Taheri et al. (2019)	16	10	62.50	37.50	0.02 um^2
Foroutan et al. (2021)	33	28	84.84	60.03	0.04 um^2
Wang et al. (2018)	32	30	93.80	66.67	0.04 um2
Proposed design	29	27	93.10	65.76	0.04 um2

Conclusion

This paper presents a Fault-Tolerant Majority Gate (FTMG) along with a comparative analysis against existing designs. The proposed design achieves higher fault tolerance while utilizing fewer device cells compared to existing approaches. The proposed design provides fault tolerance of 93.10% for Single Missing Cell Defects (SMCD) and fault tolerance of 65.76% for Double Missing Cell Defects (DMCD), also displacement defects with 100% tolerance. Since fault-tolerant circuits are essential for the implementation of large-scale logic systems, a full adder and decoder circuit has been designed using the proposed FTMG. The functionality and performance of the design have been validated through simulations using the QCADesigner 2.0.3 tool.

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Author's Contributions

Ami Patel: Conception and design: designed the proposed fault tolerant majority gate, also calculated fault tolerance based on the functionality for single and double missing cell defect, displacement defect using the tool QCA Designer. Drafting the Manuscript.

Vrushank Shah: Reviewing the manuscript, provided revision remarks.

Dipti Khurge: Provided the technical support for improvising the design results Reviewing the manuscript.

Ethics

Authors declare no competing interest.

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